

◆ Cadence OrCAD V16.5 Capture/CIS What's New

在最新版本 Cadence OrCAD Capture/CIS V16.5 版本中，新增加電路圖物件鎖定及零件報表等功能，以及在 CIS 中增加電路圖區域模擬設定及環境備份功能。

請參考以下 OrCAD V16.5 各種新功能介紹。

• **Date :** 2011 / 06 / 07

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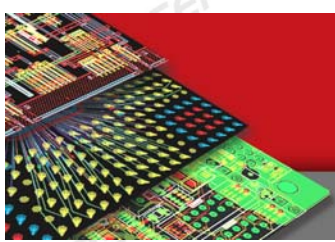
• **Revision :**

• **Version :** V16.5

• **備註:**

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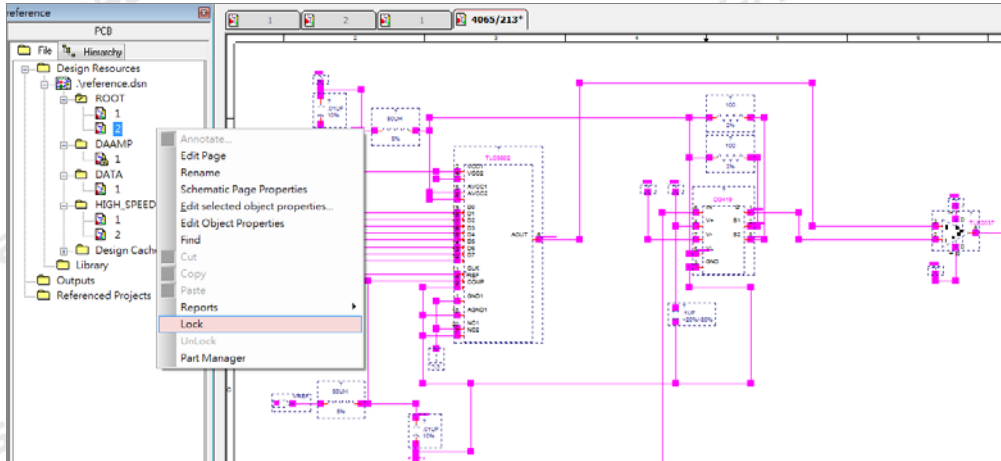
<http://www.graser.com.tw>



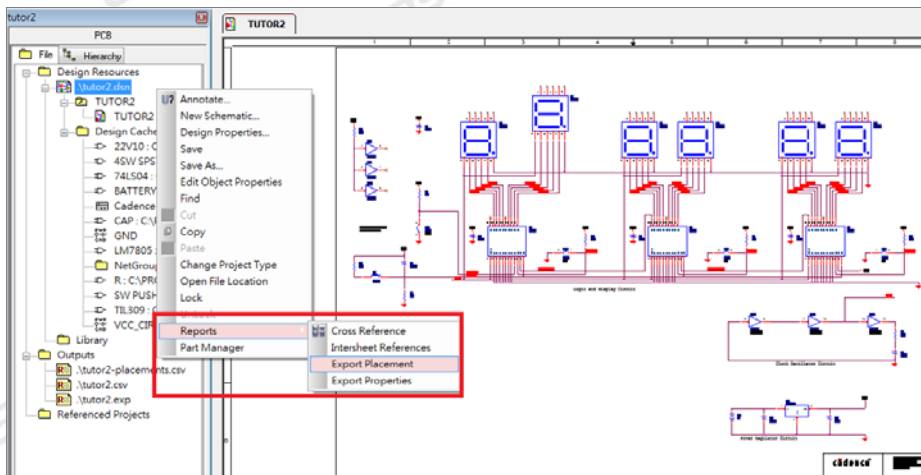
◆ OrCAD Capture V16.5 新增之功能

- Graphical Operation (GOp) Locking 電路圖物件鎖定功能

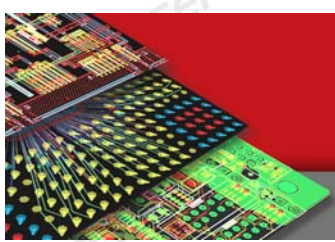
Use : By Design Setting ; By Page Setting ; By Selection Setting



- Part Placement Report 電路圖零件位置 Report



| | A | B | C | D | E | F | G | H | I |
|----|------|-----------|-------|-----------------|----------|------|------|---|---|
| 13 | | | | | | | | | |
| 14 | Item | Reference | Part | Schematic Sheet | Library | X | Y | | |
| 15 | | | | | | | | | |
| 16 | | | | | | | | | |
| 17 | 1 | BT1 | 9V | TUTOR2/T | 1 C:PROG | 13.2 | 12.3 | | |
| 18 | 2 | C1 | .01UF | TUTOR2/T | 1 C:PROG | 2.7 | 2.6 | | |
| 19 | 3 | C2 | .01UF | TUTOR2/T | 1 C:PROG | 4.5 | 6.3 | | |
| 20 | 4 | C3 | .01UF | TUTOR2/T | 1 C:PROG | 9.9 | 6.3 | | |
| 21 | 5 | C4 | .01UF | TUTOR2/T | 1 C:PROG | 15.2 | 6.3 | | |
| 22 | 6 | C5 | 100uF | TUTOR2/T | 1 C:PROG | 2.2 | 7.2 | | |
| 23 | 7 | C6 | 47UF | TUTOR2/T | 1 C:PROG | 18.7 | 10.2 | | |
| 24 | 8 | C7 | 470uf | TUTOR2/T | 1 C:PROG | 14.3 | 12.4 | | |
| 25 | 9 | C8 | 22uf | TUTOR2/T | 1 C:PROG | 16.5 | 12.4 | | |

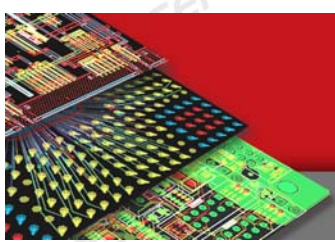


- **Generate reports for Find results** 產生物件搜尋結果報告為 CSV or HTML 檔案

| Reference | Value | Source Part | Source Library | Page | Page Number | Schematic | Zone |
|-----------|-------|-------------|----------------|--------|-------------|-----------|------|
| C1 | .01uF | CAP | C:\PROGRAM... | TUT... | 1 | TUTOR2 | 2A |
| C2 | .01uf | CAP | C:\PROGRAM... | TUT... | 1 | TUTOR2 | 2B |
| C3 | .01uf | CAP | C:\PROGRAM... | TUT... | 1 | TUTOR2 | 4B |
| C4 | .01uf | CAP | C:\PROGRAM... | TUT... | 1 | TUTOR2 | 7B |
| C5 | 100uF | CAP | C:\PROGRAM... | TUT... | 1 | TUTOR2 | 1B |

| Reference | Value | Source Part | Source Lib | Page | Page Num | Schematic | Zone |
|-----------|--------|-------------|------------|--------|----------|-----------|------|
| BT1 | 9V | BATTERY | C:\PROGR | TUTOR2 | 1 | TUTOR2 | 6D |
| C1 | .01uF | CAP | C:\PROGR | TUTOR2 | 1 | TUTOR2 | 2A |
| C2 | .01uf | CAP | C:\PROGR | TUTOR2 | 1 | TUTOR2 | 2B |
| C3 | .01uf | CAP | C:\PROGR | TUTOR2 | 1 | TUTOR2 | 4B |
| C4 | .01uf | CAP | C:\PROGR | TUTOR2 | 1 | TUTOR2 | 7B |
| C5 | 100uF | CAP | C:\PROGR | TUTOR2 | 1 | TUTOR2 | 1B |
| C6 | 47UF | CAP | C:\PROGR | TUTOR2 | 1 | TUTOR2 | 8C |
| C7 | 470uf | CAP | C:\PROGR | TUTOR2 | 1 | TUTOR2 | 6D |
| C8 | 22uf | CAP | C:\PROGR | TUTOR2 | 1 | TUTOR2 | 7D |
| D1 | TIL309 | TIL309 | C:\PROGR | TUTOR2 | 1 | TUTOR2 | 2A |

- **Net Group Support** 支援電氣線群組設定功能

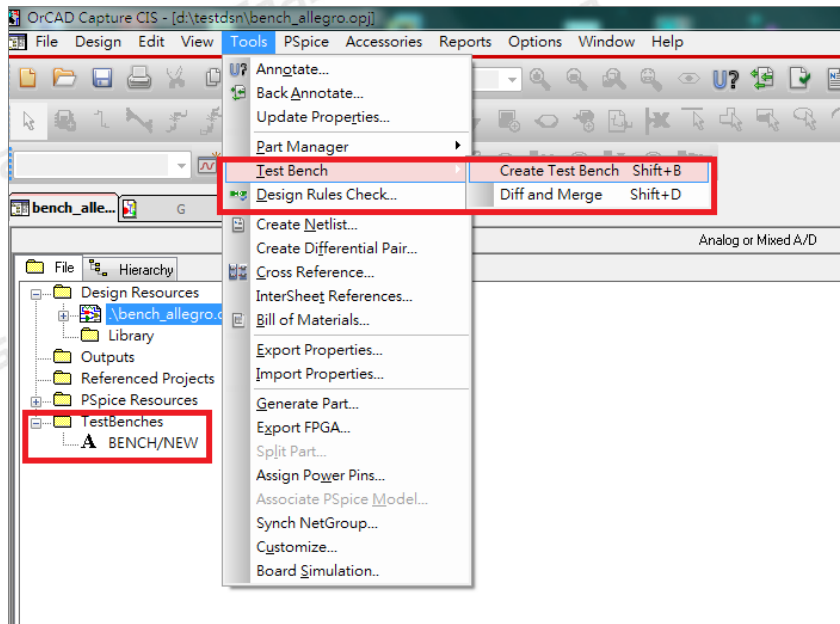


- **Separate INI Setting 備份 Capture CIS 環境設定功能**

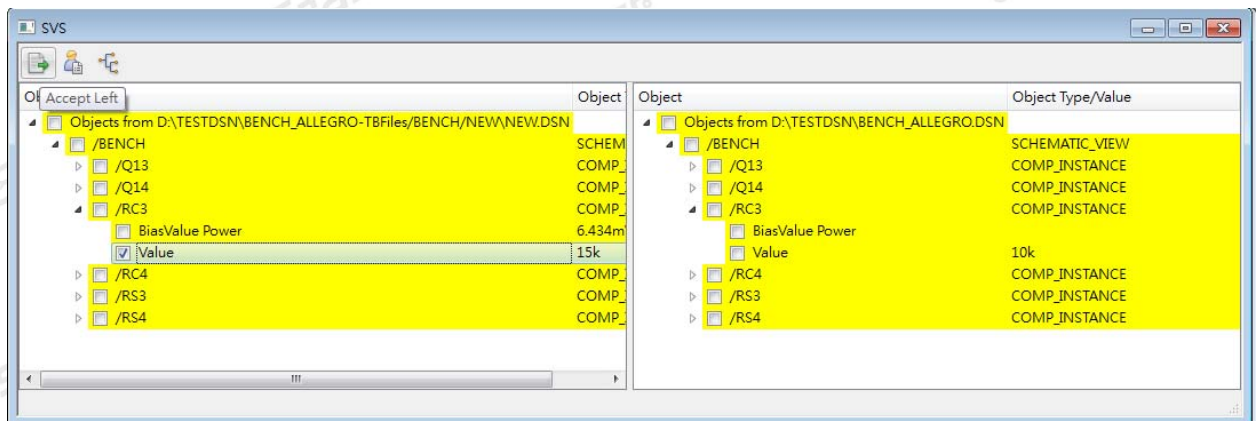
16.5 now retains the CIS INI settings in a separate back-up file. These settings are then restored during re-initialization of Capture INI.

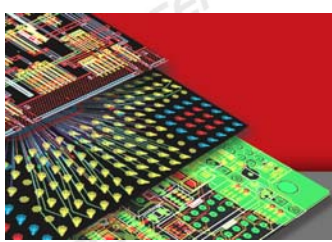
- **Partial Design Simulation 區域性模擬設定功能**

Create Test Bench



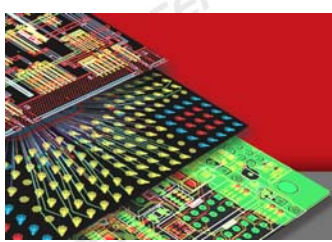
Diff and Merge





FIX CCR

| CCR ID | Description |
|---------------|--|
| CCMPR00010116 | Add Intersheet references doesn't work in Complex Hierarchy |
| CCMPR00011833 | Junction not automatically placed when it should be. |
| CCMPR00013373 | Select length of pin graphics |
| CCMPR00016310 | Simple hierarchy; intersheet refs not referring to H- block |
| CCMPR00107219 | Capture.ini switch is needed as a Registry entry like PSpice |
| CCMPR00134692 | DDB_WARN: POWER_GROUP prop. not allowed wrongly coming |
| CCMPR00136260 | Problem with netlisting the design in PSpice |
| CCMPR00145226 | placing of pictures/graphics stored in jpg/jpeg format. |
| CCMPR00207620 | Part in MISC2.OLB has incorrect pin out |
| CCMPR00226478 | generate allegro netlist if hier block has no symbol |
| CCMPR00282027 | Problem with Split Part and part graphics |
| CCMPR00299384 | Part rotation resets the text to default position |
| CCMPR00380714 | Ability to have Power pin set to Not Connect |
| CCMPR00382860 | Display parts and nets in different colors |
| CCMPR00428261 | spaces at end of pin name Could not create new pin inst library correction utility |
| CCMPR00461052 | command line arguments for cis.exe |
| CCMPR00568273 | documentation of variables in Capture.ini |
| CCMPR00585904 | Find a schematic page with help of nets |
| CCMPR00591847 | Add Intersheet References does not work on simple H design. |
| CCMPR00593076 | Cannot redisplay an invisible OFFPAGE connector's name |
| CCMPR00607432 | error code SPCODD-409 need to be documented |
| CCMPR00617784 | Trying to open page 2 of the design Capture crashes |
| CCMPR00620303 | Enhancement:Shortcut key for "Select Entire Net" |
| CCMPR00621054 | Renamed net in netlist isolates components from the rest of the net. |
| CCMPR00623218 | display pin names associated with a net in net Properties |
| CCMPR00623777 | Place Wire not working correctly |
| CCMPR00627048 | entanglement to have new check option for DRC0042 |
| CCMPR00627232 | incorrect Rinf netlist creation in Capture |
| CCMPR00629008 | enhancements for find command |
| CCMPR00631910 | Capture hangs when working with search option |
| CCMPR00634749 | Enhancement to change back the way arc was created earlier before orcad 16.2 |
| CCMPR00636156 | Unable to convert SDT Schematic to Capture Design |
| CCMPR00636585 | Rotating components in Capture reset property position |
| CCMPR00637768 | Enhancement to assign different colors to different net based on a unique property |



- CCMPR00641406 SPB 16.2 default print option changed to Inst mode
- CCMPR00642095 Ability to disable the Pop-Up description of elements
- CCMPR00642436 Save As symbol in part editor is not working fine
- CCMPR00643330 path to allegro.cfg in opj file
- CCMPR00650541 usage of PACK_IGNORE property
- CCMPR00652200 How do I move the Find Window dialog to the right side with the Place Part dialog?
- CCMPR00653784 Off-page connector name change to internal starting like "I1234555"
- CCMPR00653902 Enhancement ?Print Option? setting in Capture.ini file
- CCMPR00657131 Reference used in netlist formatter creates empty output and no warnings/errors
- CCMPR00657180 Enhancement:Tooltip for DRC markers
- CCMPR00657640 Zoom using Ctrl+Scroll mouse is different from Zoom using key " I "
- CCMPR00663260 Enhancement: ALG0051 message should be more specific
- CCMPR00666186 Enhancement FishEye functionality in Variant View Mode
- CCMPR00668081 Capture Crash during Edit options
- CCMPR00668799 Placing specific part crashes OrCAD Capture
- CCMPR00672345 Remove tutorial for Orcad Layout or put it at the end in flowtut document
- CCMPR00673410 search by net name is finding electrical
- CCMPR00674555 If the DSN filename contains spaces; autobackup will not write any DBK files to
- CCMPR00679960 Capture crashes from diff pair setup menu
- CCMPR00687074 Part disappears when you open it
- CCMPR00687354 Not able to create allegro netlist 228 ERROR(SPCODD-228): Cannot package
- CCMPR00694139 Case difference of net and bus while generating FPGA netlist
- CCMPR00696534 Pin Visibility check box doesn't work while creating part from spreadsheet editor
- CCMPR00703905 Need Hot Fix number Info on Help >> About
- CCMPR00706729 Import properties fails with ERROR [IMP0020]
- CCMPR00710859 Unable to create Diff Pair from Autosetup
- CCMPR00712299 Internal application error while creating new design
- CCMPR00716212 PACK_SHORT property gives package error for visible POWER pins
- CCMPR00722346 DRC checks for mismatches in labeling Net

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